National Institute of Electronics and Information Technology (NIELIT)
Dwarka, New Delhi

राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, द्वारका, नई दिल्ली -110077

DETAILED ADVERTISEMENT
(Advt. No. NHQ-35/24/2026-NIELIT [3175427])

NIELIT requires the following person purely on contract basis on consolidated remuneration initially for a period of one year: -

1. Name of Position	**Team Lead (VLSI Design)**
Position Code	**2506-TLVD**
No of Position	**05 (Five)** NIELIT Corporate Office
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 95,000/- P. M.
Eligibility Criteria and Experience	**Essential:** Bachelor's/Master's/PhD in Electronics & Communication Engineering, VLSI Design, or related field. **Experience:** 4 years of relevant experience in industry/academia/R&D Organization **Note**: Duration of PhD will be counted as R&D experience. **Job description:** **Key responsibilities include:** • Lead the design and development of reusable IP blocks using open-source EDA tools, and oversee their validation and documentation. • Drive end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Lead a cross-functional team for content creation, tool integration, and platform delivery. • Design and develop audio-visual content and labs for RTL-to-GDSII flow using open-source EDA tools. • Oversee integration of open source EDA tools and design flows into the web-based EdTech platform. • Collaborate with academic and industry experts to develop and update modular, job-ready curricula. • Mentor junior engineers and trainers; drive knowledge sharing and skill development. • Facilitate community-building, including forums, bootcamps, and mentorship initiatives. • Ensure quality, track learner feedback, and implement continuous improvements in training and platform features. **Preferred Skills** • Strong understanding of instructional design principles and curriculum frameworks (AICTE, NEP, etc.). • Familiarity with LMS platforms (e.g., Moodle, Canvas) and digital content formats (SCORM, MP4, PDFs). • Experience working with academic institutions or government skilling programs. • Excellent organizational, communication, and mentoring skills.
2. Name of Position	**VLSI Design Expert/ Junior VLSI Engineer**
Position Code	**2506-VLSIDE**
No of Position	**02 (Two)** NIELIT Corporate Office

Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 40,000/- P.M

Eligibility Criteria and Experience	**Essential: -** Masters in Electronics & Communication, Electrical Engineering, VLSI Design, or related field.
	OR Bachelor in Electronics & Communication, Electrical Engineering, VLSI Design, or related field with one year experience
	
	Job description:
	Key responsibilities include:
	
	• To assist in design and development of reusable IP blocks using open-source EDA tools, their validation and documentation
	
	• Design and develop in-depth academic and practical content in one or more of the following domains:
	  ○ **RTL Design & Integration**
	  ○ **Physical Design**
	  ○ **Synthesis and STA**
	  ○ **DFT and ATPG**
	  ○ **Analog and Mixed-Signal Design**
	  ○ **Digital and Analog Design Verification**
	  ○ **Standard Cell and PDK-based design**
	• Create reproducible design labs and projects using open-source tools such as:
	  ○ **Magic, KLayout, Yosys, OpenROAD, Ngspice, Xschem, Netgen, GHDL, Verilator, etc.**
	• Develop and document exercises, assignments, and mini-projects for each design domain.
	• Record demos or work with AV teams to create training videos and tutorials.
	• Collaborate with content designers, platform developers, and trainers to align content with platform capabilities.
	• Test and validate open-source flows with actual design examples and student-level reproducibility.
	• Mentor junior engineers, interns, and trainers when needed.
	
	Preferred Skills
	• Prior teaching, curriculum development, or instructional design experience.
	• Exposure to cloud-based VLSI design environments or FPGA-based learning kits.
	• Knowledge of modern teaching aids – LMS platforms (e.g., Moodle), video content creation, screen recording tools.
	• Strong written and verbal communication skills.

3. Name of Position	**Senior Trainers (VLSI Design)/ Senior VLSI Engineer**
Position Code	**2506-STVD**
No of Position	01 **(One)**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65000/- P.M
Eligibility Criteria and Experience	**Essential:** B.Tech/M.Tech in ECE, EE, VLSI Design or related field. **Experience**: 3 years of relevant experience in industry/academia/R&D Organization **Note:** Duration of PhD will be counted as R&D experience

	Job description: • To assist in design and development of reusable IP blocks using open-source EDA tools, their validation and documentation • To develop end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Conduct Train-the-Trainer (ToT) programs for faculty and academic partners. • Deliver workshops, bootcamps, and webinars for students, faculty, and professionals. • Use open-source tools (e.g., Yosys, Magic, OpenROAD, KLayout, Ngspice, Verilator, Xschem) to conduct hands-on sessions. • Help participants with design challenges, practical labs, and capstone projects. • Serve as a point of contact for 10–20 assigned academic institutions. • Guide partner faculty in adopting and integrating course content into their curricula. • Provide ongoing academic mentorship and resolve technical or pedagogical queries. • Ensure learning continuity via LMS, forums, or online sessions. • Collect feedback, performance data, and learning outcomes. • Work with the central content and platform team to suggest improvements. • Assist in conducting assessments, certifications, and project evaluations. • Help users onboard and use the open-source chip design platform effectively. • Report technical issues and contribute to documentation and FAQs. • Maintain a knowledge base and support structure for learners and faculty.
4. Name of the Position	**Junior DevOps Engineer**
Position Code	**2506-DOE**
No. of Position	**01 (One)**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 30 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 25,000/- P. M.
Eligibility Criteria and Experience	**Essential:** Bachelor's or Master's degree in Computer Science, IT, or a related field. **Note for Final-Year Students:** Candidates in their final semester are welcome to apply. If selected, appointment is subject to the submission of a provisional degree certificate at the time of joining. **Job description:** Key responsibilities include: • Manage Kubernetes-based infrastructure on AWS EKS • Manage CI/CD pipelines for automated testing, building, and deployment • Ensure high availability, reliability, and performance of services on production • Implement monitoring, logging, and alerting using tools like Prometheus, Grafana, ELK stack, or CloudWatch

	• Manage secrets, certificates, and access controls securely • Define and maintain infrastructure as code using Terraform or AWS CloudFormation • Optimize deployment processes, cost, and scalability across environmentsManage user authentication, data security, and access control mechanisms. • Set up storage solutions for lab files, simulation data, and course materials. • Collaborate with platform developers, instructional teams, and VLSI engineers to ensure infrastructure readiness. **Preferred Skills** • Expertise in Kubernetes (EKS) cluster management and container orchestration • Strong knowledge of AWS services (EKS, EC2, RDS, S3, IAM, CloudWatch, etc.) • Proficiency in scripting (Bash, Python, or similar) • Experience with CI/CD tools (GitHub Actions, Jenkins, or similar) • Knowledge of Docker, Helm, and infrastructure monitoring tools • Experience implementing security best practices (firewalls, IAM roles, VPC setups) Strong problem-solving and analytical skills. • Excellent communication and team collaboration abilities.
5. Name of the Position	**Junior Full Stack Engineer**
Position Code	**2506-FSE**
No. of Position	**05 (Five)**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 30 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 25,000/- P.M
Eligibility Criteria and Experience	**Essential:** Bachelor's or Master's degree in Computer Science, IT, or a related field. **Note for Final-Year Students:** Candidates in their final semester are welcome to apply. If selected, appointment is subject to the submission of a provisional degree certificate at the time of joining. **Job description:** **Key responsibilities include:** • Develop and maintain scalable web applications using Java, Spring Boot, and React • Design and implement RESTful APIs and integrate them with the frontend • Use Monaco Editor to support advanced code-editing features on the platform • Manage frontend components with React Bootstrap • Package and manage backend services using Maven • Work with DevOps to ensure CI/CD and containerization best practices • Write unit and integration tests to ensure code quality • Perform code reviews and maintain high coding standards • Debug production issues and ensure platform uptime and performance **Preferred Skills** - Strong proficiency in Java and Spring Boot - Strong command over React and modern JavaScript/TypeScript - Experience with Monaco Editor integration in React apps - Familiarity with Maven, REST APIs, Git, and CI/CD

	pipelines - Understanding of microservices architecture and containerized deployments (Docker/Kubernetes) - Experience working with cloud services on AWS
6.Name of the Position	**Project Assistant-VLSI**
Position Code	**2506-VTE**
No. of Position	**21 (Twenty One)**
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 30 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs.25000/- P.M.

Eligibility Criteria and Experience	**Essential:** Bachelor's or Master's degree in Electronics & Communication Engineering, Electrical Engineering, VLSI Design, or related field.
	
	Note for Final-Year Students: Candidates in their final semester are welcome to apply. If selected, appointment is subject to the submission of a provisional degree certificate at the time of joining.
	
	Desirable Skills:
	• Strong academic background in Digital Electronics, Verilog, CMOS Design, and Semiconductor Fundamentals.
	• Familiarity with ASIC design flow and FPGA-based development.
	• Exposure to open-source EDA tools such as Yosys, OpenROAD, Magic, KLayout, Ngspice, Verilator, and Xschem.
	• Understanding of Linux environments and scripting basics (Python/Shell).
	• Knowledge of RISC-V architecture and SoC design concepts.
	• Good analytical, problem-solving, and communication skills.
	
	Job description:
	Key responsibilities include:
	• To assist in design and development of reusable IP blocks using open-source EDA tools, their validation and documentation
	• Design and develop in-depth academic and practical content in one or more of the following domains:
	  o **RTL Design & Integration**
	  o **Physical Design**
	  o **Synthesis and STA**
	  o **DFT and ATPG**
	  o **Analog and Mixed-Signal Design**
	  o **Digital and Analog Design Verification**
	  o **Standard Cell and PDK-based design**
	• Create reproducible design labs and projects using open-source tools such as:
	  o **Magic**, **KLayout**, **Yosys**, Openlane, **OpenROAD**, **Ngspice**, **Xschem**, **Netgen**, **GHDL**, **Verilator**, etc.
	• Develop and document exercises, assignments, and mini-projects for each design domain.
	• Record demos or work with AV teams to create training videos and tutorials.
	• Collaborate with content designers, platform developers, and trainers to align content with platform capabilities.
	• Test and validate open-source flows with actual design

	examples and student-level reproducibility. • Conducting online/offline training programs, workshops, hackathons etc.

General Terms & Conditions:

1. The qualification of candidates must be from Govt. University or Govt. recognized University/Institutions.
2. Applicants with last semester result awaited or incomplete degrees are not eligible to apply.
3. Cut-off date for calculating age and experience shall be the date mentioned in **Walk-in-Interview Advertisement.**
4. Non-refundable Registration Fee of ₹500/- per position to be deposited through online mode. The Candidates may deposit registration fee in the account of NIELIT in the given Bank account on or before Document Verification & Walk-in-Interview date.

Name of the office	National Institute of Electronics and Information Technology, New Delhi
Bank Account Number	604820100000012
Bank Name	Bank of India
IFSC Code	BKID0006048

Venue for Document Verification and Interview:	National Institute of Electronics & Information Technology, NIELIT Bhawan, Plot No. 3, PSP Pocket, Sector-8, Dwarka, New Delhi-110077
Document Verification	09:30 AM to 11:00 AM
Interview	11.00 A.M. onwards

5. Applications without requisite application fee (Rs. 500/-) shall be summarily rejected at any stage of Document Verification and Walk-in-Interview.
6. Applicants are requested to fill Application Form and attach all the required (self-certified) documents including Payment Receipt.
7. The Applicants who report at NIELIT HQ before 11:00 AM shall be considered for Document Verification.
8. Applicants are requested to come with Original Documents for Document Verification.
9. Document Verification (based on the documents produce by applicant with application form) and Walk-in Interview is to be done as per date mentioned in the advertisement.
10. Only those candidates who clears Document Verification will be allowed to appear in Walk-in-Interview.
11. Applicants are requested not to send Application Form thru Post or any other medium to NIELIT HQ.
12. NIELIT has the right to accept or reject the application without assigning any reason thereof.
13. Applicants are advised to visit the website of NIELIT **http://nielit.gov.in/recruitments** for any updates.
14. No separate communication shall be made in any other form.
15. The number of vacancy is tentative and liable to change as per the requirement of NIELIT.
16. The Remuneration mentioned above is consolidated salary (CTC). The selected candidate will not be paid any other financial benefits like Medical, HRA, Transport etc. except the consolidated salary.
17. Selection of candidate for appointment to the above mentioned position will be based on the performance of the candidates in the walk-in-interview and as found eligible as per prescribed criteria.
18. The selected candidate will be engaged purely on contract basis initially for a period of one year, which may be extended depending upon the requirement and performance of the candidate.
19. The offer of appointment for the selected candidate will be subject to verification of original certificates/testimonials at the time of interview and completeness of other formalities.
20. NIELIT will also create a panel for contractual deployment and the candidates will be selected for deployment on contract from the panel as and when required.
21. Only those candidates who deposit requisite registration fee of Rs. 500/-, clear document verification and successful interaction will be empaneled.
22. Empanelment means the shortlisted candidates will be in the panel of NIELIT for one year. They may be deployed in specific Govt. department/ NIELIT as per department requirements purely on contract basis. Mere empanelment does not ensure deployment in any department nor provide any right to candidate to claim for deployment.
23. Empaneled candidates list will valid for one year from the date of result declaration.
24. Candidates will not be entitled to claim any TA/DA for appearing in Interview.
25. Canvassing/trying to influence NIELIT employees to secure the job in any manner shall disqualify the candidate.
26. In the case of any legal dispute, the jurisdiction shall be Delhi.