इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY

रा.इ.सू.प्रौ.सं NIELIT

SoC Teamup

# NATIONAL INSTITUTE OF ELECTRONICS & INFORMATION TECHNOLOGY NOIDA

INTERNSHIP/TRAINING PROGRAM

VLSI DESIGN FLOW
(RTL TO GDS-II)(ONLINE MODE)

# INFORMATION BROCHURE

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MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY
सत्यमेव जयते

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SoCTeamup

**NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY, NOIDA**

**Name of Group:** Centre of Excellence in Chip Design at NIELIT NOIDA in association with SoCTeamup Semiconductors Pvt Ltd as industry partner

**Name of Course**: Internship/Training Program on VLSI Design flow (RTL to GDS-II) **(Online Mode)**

**Objective:** The Internship/Training in Program on VLSI Design flow (RTL to GDS-II) (Online Mode) aims to provide a comprehensive overview of Very Large Scale Integration concepts, covering digital design methodologies, ASIC and FPGA technologies, physical design, and testing. Participants will gain hands-on experience with open source **EDA toolsuite**, explore power-efficient design strategies, and delve into emerging trends. The course emphasizes practical applications through project work and offers insights from industry experts who have delivered **30+ chip tapeouts** for top design houses like Intel, STMicroelectronics, NXP to name a few, enabling a foundational understanding of VLSI principles and practices in a condensed timeframe.

**Duration: 30 Days/ 06 Weeks (90 Hours) (3 hrs/day) (1hr Theory, 1hr Practical, 1hr additional Lab access)**

**Mode of Delivery:** Online mode

**Eligibility:** B.Tech/M.Tech/B.Sc/M.Sc / or (Diploma in relevant field with min Two Year Industry Experience)

**Note**: Research Scholars, Faculty members and **Industry professionals** can also enroll

**Prerequisites: -**

1. Basic knowledge of digital circuits and logic gates.
2. Familiarity with a hardware description language (HDL) such as Verilog or VHDL
3. Familiarity with a Unix/Linux environment and command-line interface

**Course Fees: Rs. 2700/- (incl. GST)**

**Registration Process:** Candidates have to apply in prescribed application form through online registration portal https://regn.nielitvte.edu.in/ or through Android App "**NIELIT Kaushal Setu**". The duly filled form along with the course fees has to be submitted in online mode through the above link. The Fees deposited is Non-Refundable.

**Topics to be Covered**

- **Overview of VLSI Design Flow**
- **Hardware Modeling: Introduction to Verilog-I**
- **RTL Synthesis**
- **Static Timing Analysis**
- **Basic Concepts for Physical Design**
- **Floorplanning,clock tree synthesis,routing**

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Deputy Director/Scientist 'C'
& OIC, CoE Chip Design Noida Centre

| Week No. | Lecture No. | Lecture Title | Concepts Covered |
|---|---|---|---|
| Week 1 | Module 1 | Basic Concepts of Integrated Circuit - I | This lecture gives a historical perspective on integrated circuits, trends of scaling, and Moore's law. It also describes the structure of an integrated circuit and the role of photolithography in its fabrication. Basic concept of CMOS,CMOS logic design. |
| | Module 2 | Overview of VLSI Design Flow - II | This lecture describes the differences between a high-level description of a design and its register transfer level (RTL) description. Further, it describes the system-on-chip (SoC) design methodologies and how a design can be composed by assembling various intellectual properties (IPs). Further, it describes generating RTL using behavioral synthesis, various trade-offs involved in this process, and the associated challenges. |
| | Tutorial 1 | Introductio n to LINUX | This tutorial describes creating a LINUX environment using Windows Subsystem for Linux(WSL) in a Windows operating system. Then, it describes a few essential UNIX commands. |
| Week 2 | Module 3 | Overview of VLSI Design Flow | This lecture describes the role of logic synthesis in VLSI design flow. It describes various terminologies associated with netlists generated by a logic synthesis tool. Further, it briefly describes various tasks involved in logic synthesis, such as RTL synthesis, logic optimization, and technology mapping. |
| | Module 4 | Overview of VLSI Design Flow | This lecture describes the role of physical design in VLSI design flow. It briefly explains various design tasks involved in physical design, such as chip planning, placement, clock tree synthesis (CTS), global routing, and detailed routing. Further, it highlights the significance of optimizations, iterative flows, and the challenges of achieving design closure. |
| | Module 5 | Overview of VLSI Design Flow | This lecture describes the significance of various design verification methods, such as simulation, formal verification, static timing analysis, and physical verification. |
| | Tutorial 2 | Introductio n to TCL | This tutorial introduces the tool command language (TCL) and its various commands. TCL is widely used in VLSI design flow to give inputs to the EDA tools and automate design flows. |

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| Week No. | Lecture No. | Lecture Title | Concepts Covered |
|---|---|---|---|
| Week 3 | Module 6 | Hardware Modeling: Introduction to Verilog-I | This lecture highlights the distinct features of hardware description languages (HDL) compared to other high-level programming languages. Further, it introduces the Verilog language, especially describing lexical rules, identifiers, four-valued data, Verilog nets, variables, vectors, and arrays. |
| | Module 7 | Hardware Modeling: Introduction to Verilog-II | This lecture describes various Verilog language constructs, especially modules, ports, instantiation, and parameterized modules. It also explains operators, expressions, conditional blocks, loop controls, initial blocks, always blocks, functions, and tasks. It also describes the differences between continuous, blocking, and non-blocking assignments. |
| Week 4 | Module 8 | RTL Synthesis Part I | This lecture explains the role of RTL synthesis in VLSI design flow and its various tasks, such as lexical analysis, parsing, elaboration, translation, and optimization. It highlights synthesizable and non-synthesizableconstructsinVerilog. Additionally, it explains the synthesis of assign statements, conditional blocks, always block, inference of flip-flops/latches, and synthesis of blocking and non-blocking assignments. |
| | Module 9 | Logic Optimization : Part I | This lecture highlights the role of logic optimization in VLSI design flow. It discusses two-level logic minimization for incompletely specified Boolean functions. First, it explains exact logic minimization using Quine's theorem and prime implicant tables. Then, it briefly describes heuristic two-level logic minimization. |
| | Tutorial 3 | Synthesis using Yosys-I (Tentative) | Practical Session |
| | Module 10 | Logic Optimization : Part II | This lecture discusses multi-level logic minimization for a Boolean logic network using transformations such as simplify, eliminate, substitute, and extract. It also highlights the opportunities and challenges of optimizing using an algebraic model compared to a Boolean model. |
| | Tutorial 4 | Synthesis using Yosys-II (Tentative) | Practical Session |

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| Week No. | Lecture No. | Lecture Title | Concepts Covered |
|---|---|---|---|
| Week 5 | Module 11 | Static Timing Analysis | This lecture explains the basic concepts and motivation for static timing analysis (STA) in VLSI design flow. It describes the problem of zero clocking and double clocking in a synchronous circuit and derives constraints for avoiding these problems. Further, it explains how an STA tool models these constraints using arrival time and required time. |
| | Module 12 | Static Timing Analysis | This lecture explains the mechanics of static timing analysis (STA), which will help designers analyze the timing reports generated by the STA tools and take corrective measures if needed. Specifically, it describes various kinds of paths in a circuit from the perspective of STA, timing graph, delay calculation, arrival/required time calculation, and slack computation. |
| | Module 13 | Static Timing Analysis | This lecture explains two types of slew propagation in static timing analysis (STA): graph-based analysis (GBA) and path-based analysis (PBA). It also explains accounting for variations in STA, using margins, multi-mode multi-corner (MMMC) analysis, and on-chip variations (OCV) derating factors. |
| | Tutorial 5 | Static Timing Analysis using OpenTimer | Practical Session |
| Week 6 | Module 14 | Constraints I | This lecture discusses the role of constraints, typically written in synopsys design constraints (SDC) format, in VLSI design flow. Further, it explains how these constraints can be specified for clock sources and their attributes, such as latency, uncertainty, and transition. |
| | Module 15 | Technology Mapping | This lecture explains the role of technology mapping in VLSI design flow. It illustrates various trade-offs involved in technology mapping, its opportunities, and challenges. |
| | Module 16 | Basic Concepts for Physical Design | This lecture describes some concepts that are essential in appreciating physical design tasks. It discusses signal integrity issues, including dynamic delay variations and crosstalk noise. It also explains the antenna effect and information contained in library exchange format (LEF) files. |

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| Week No. | Lecture No. | Lecture Title | Concepts Covered |
|---|---|---|---|
| Week 6 | Module 17 | Floorplanning, Clock tree synthesis, routing | This lecture describes various tasks involved in clock tree synthesis (CTS), including its target of minimizing the clock skew. It discusses various global clock distribution networks and local clock distribution networks. It also covers tasks involved in routing, including global routing, detailed routing, and post-routing optimizations. |
| | Tutorial 6 | Flow automation using Qflow | Practical Session |

* There will be 2 Hours Session per day in **online mode**.

**Mode of Payment:** Fees can be paid either by debit/credit card or in any online mode.

For any queries and more details please contact on **8218724641/9811295181**

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## Course Venue: Online

NIELIT NOIDA, IETE NOIDA Centre Building, PS-1D, Behind Brahampurtra Shopping Complex Sector 29, Noida, Uttar Pradesh 201301

**Registration Link:**

https://regn.nielitvte.edu.in
or
Through Android App "**NIELIT Kaushal Setu**"

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