

**INTERNSHIP/TRAINING PROGRAM ON FUNCTIONAL VERIFICATION WITH
SYSTEM VERILOG AND UVM DURATION : 120 HOURS****FUNCTIONAL VERIFICATION WITH SYSTEM
VERILOG AND UVM - 8 Weeks Offline Course****(5 DAYS /Week : 3hrs /Day)****Objective**

The objective of the course is to take a lab oriented hands on practical approach for learning FUNCTIONAL VERIFICATION WITH SYSTEM VERILOG AND UVM via examples with more complete discussion. Numerous examples are provided to Learn and Re-Learn

B.E/B.Tech./M.Sc./M.Tech

Eligibility**Prerequisite**

- Basic Knowledge of Digital Design
- Basic knowledge of oops

Rs.16992/- incl. GST & all other charges.

Course Fees**Certificate**

Certificate will be provided to the participants, based on minimum 75% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

- Instructor-led live classes.
- Instructor-led hands-on lab sessions.
- Content Access through e-Learning portal
- Assessment and Certification .

Methodology**How to Apply**

Step-1: Read the course structure & course requirements carefully. **Step-2:** Visit the Registration portal and click on apply button.

Step-3: Create your login credentials and fill up all the details, see the preview and submit the form.

Step-4: Login with your credentials to verify the mobile number, email ID and then upload the documents, Lock the profile and Pay the Fees online, using ATM-Debit Card / Credit Card / Internet Banking / UPI etc.

Course Content

Week	Topic	Week	Topic
Week01	Introduction to Verilog: • Origins, Overview, Need and Importance • Verilog Data types. • Basic Verilog example .	Week05	Coverage • Understanding Coverage • Methodology • Code Coverage • Types of code coverages.
Week02	Introduction to System Verilog • Origins, Overview, Need and Importance • Introduction System Verilog Verification environment . • Data types In system Verilog. • Arrays: □ Array Handling, Dynamic Array, Associative Array, Queues in System Verilog	Week06	Introduction to the AMBA APB Protocol Sharing of specs Understanding the signals .
Week03	Task and functions in system verilog. • Void function in System Verilog. • Different type of loops in SV .	Week07	Introduction to Universal Verification Methodology (UVM) • Coverage-Driven Verification (CDV) • UVM testbenches and environments • Verification components: 1. Data Item (Transaction) 2. Driver (BFM) 3. Sequencer 4. Monitor
Week04	Randomization • Introduction Week07 • Randomization in real world. • Randomization in System Verilog. • Random variables	Week08	Project

Course Coordinator

Prashant Pal
Deputy Director/Scientist 'C' &
OIC, CoE Chip Design Noida Centre